PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10015169	10/23/2001	~~257~~ 345	~~64~~ 98	~~2816~~ 2675	~~STARR~~ Anyaso Lambert

**APPLICANTS: Kawahata Ken; Yamada Yukimitsu;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 2000-324496 10/24/2000
JAPAN 2001-208160 07/09/2001

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	☐ yes ☐ no	9281-4195	
Verified and Acknowledged Examiners's intials			

TITLE : Shift register circuit including first shift register having plurality of stages connected in cascade and second shift register having more stages

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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